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Multilevel Current Waveform Generation for Renewable Power System

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Abstract— In this paper we are using a new circuit configuration of single phase multilevel Current Source Inverter (CSI). With this new topology, we can generate the multilevel current waveform from a single DC (Direct Current) power source. A basic H-bridge CSI working as a main inverter generates a multilevel current waveform in cooperation with inductor cells connected in parallel as auxiliary circuits. In order to control the intermediate level of the multilevel output current waveform a controller is needed. Three level shifted multicarrier based sinusoidal PWM (Pulse Width Modulation) techniques are used in the controller and found the best technique to this new configuration. A five level Pulse Width Modulation inverter configuration, with chopper based DC current source is simulated using Matlab simulation software.

Index Terms— H-bridge CSI, Inductor cell, Logical Operations, Modulation Index, PWM strategies, Total Harmonic Distortion, Transient Period.

1 INTRODUCTION

IN THE PAST century, global surface temperatures have increased at a rate near 0.6◦C/century because of global warming caused by effluent gas emissions and increases in CO2 levels in the atmosphere[1], [2]. The problems with energy supply and use are related not only to global warming but also to such environmental concerns as air pollution, acid precipitation, ozone depletion, forest destruction, and radioactive substance emissions. To prevent these effects, some potential solutions have evolved including energy conservation through improved energy efficiency, a reduction in fossil fuel use and an increase in environmentally friendly energy supplies. Recently, energy generated from clean, efficient and environmentally friendly sources has become one of the major challenges for engineers and scientists [3], [4], [5], [6], [7]. In distributed power generation application, as most renewable energy sources, such as PhotoVoltaic (PV) systems, deliver DC (Direct Current) power; the generated power must be converted to ac power and is fed into the grid through grid connected inverters [8], [9], [10]. Recent development of high performance semiconductor power switches such as MOSFETs and IGBTs increases the research interest in high power converters, such as multilevel Voltage Source Inverter (VSIs) and its dual, multilevel Current Source Inverter (CSIs)[11], [12], [13]. Various international standards, like IEEE-1547, IEEE-929, and EN-61000-3-2, impose requirements on the inverter's output power quality, i.e., harmonic currents and Total Harmonics Distortion (THD) of the output current. Multilevel CSI is one of the effective solutions to tackle such problems. Control of the grid connected CSI is comparatively simpler than its Counterpart, VSI. A grid connected CSI can buffer the output current from the grid voltage fluctuation, generates a predetermined current to the power grid without AC current feedback loops, and can achieve a high power factor operation. Its output current is less affected by a grid voltage, and the CSI has inherent short circuit protection abilities [9], [10].

Few topologies of the multilevel CSIs have been proposed by researchers and engineers. One of which is the multilevel CSI, obtained by applying a multicell topology of the CSI (or multirating inductor multilevel CSI [14]), which is a dual converter of a flying capacitor based full bridge multilevel VSI [15]. However, this topology has a drawback with its bulky intermediate inductors and complexity for balancing control of the intermediate level currents. Some control methods have been proposed for balancing control of the intermediate level currents, but very large in size of the intermediate inductors (100 mH) are still used. These cumbersome inductors will be costly and limit the application of the inverter.

Bai and Zhang [14] presented the configuration of a single rating inductor multilevel CSI that is the dual structure of an improved diode clamped multilevel VSI. Noguchi and Suroso[16], [17] presented a common emitter configuration of the multilevel CSI obtained by connecting two level CSI modules in parallel with the three level common emitter CSI. This configuration has a great advantage over conventional approaches because all of the power switches are connected at a common emitter point or an identical potential line. This topology needs only a single isolated gate drive circuit to drive all power switches of the inverter; hence, the complexity of the gate drive circuits can be moderated. Unfortunately, the requirement of many split DC current sources is an apparent disadvantage of this topology.

This paper uses a new circuit configuration of the multilevel CSI. In this new topology, a basic H-bridge CSI, working as a main inverter circuit, is connected in parallel with inductor cells working as auxiliary circuits. The inductor cells generate the intermediate levels of the multilevel output current waveform, with no additional external DC power sources. A simple proportional integral controller is applied to control the

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intermediate level currents of the multilevel output waveform [18]. Three level shifted multicarrier based sinusoidal PWM techniques are used in the controller and found the best PWM technique to this new configuration. The usage of logical operations in generating gate pulses results in reduced transient period.

2 Working Principle and Circuit Configuration

The five level CSI configurations with chopper based DC current source are shown in the Fig. 1. The power source can be batteries, PV modules, a fuel cell, or a rectifier. Here a DC current source is obtained by connecting a chopper with the smoothing inductor Li. The chopper consists of a controlled switch (Q_C) which regulates the DC current flowing through the smoothing inductor as the DC input current I_{Li} and it is given to the H-bridge. A free-wheeling diode (D_F) is used to keep continuous current flowing through the smoothing inductor.

The new configuration of the multilevel CSI can be obtained by connecting the H-bridge CSI in parallel with a single or more inductor cells. A five level CSI configuration is obtained by connecting a single inductor cell, a nine level CSI configuration is achieved by connecting two inductor cells in parallel with the main three level H-bridge CSI. The inductor cell circuit is composed of four unidirectional power switches Q_{C1}, Q_{C2}, Q_{C3}, and Q_{C4}, and an inductor L_C connected across the cell circuit. The inductor cells generate intermediate level currents of the multilevel output waveform from the basic three level current of the H-bridge CSI. It utilizes the charging and the discharging operation modes of the inductor.

The relation between the level number of the output current waveform (M) and the number of the inductor cells (N) can be formulated as follows:

$$M = 2^{(N+1)} + 1 \tag{1}$$

For M-level CSI, if the DC current source of the main H-bridge CSI is assumed to have amplitude I, the current flowing through the Nth inductor cell $I_{Lc(i)}$ is expressed as follows:

$$I_{L_{c(i)}} = \frac{I}{2^i}$$

$$\text{Where i = 1, 2, 3…N.} \tag{2}$$

The output current levels of the five level CSIs are $+I$, $+I/2$, 0, $-I/2$, and $-I$. For the nine level CSI, the output waveform has $+I$, $+3I/4$, $+I/2$, $+I/4$, 0, $-I/4$, $-I/2$, $-3I/4$, and $-I$ current levels. Table 1 lists the switching states of the five level CSI.

The charging operation mode of the inductor L_c is conducted when the switches Q_{C1} and Q_{C3} are turned on, while the switches Q_{C2} and Q_{C4} are turned off. A current $I_{Lc} = I/2$ flows through the power switches Q_{C1} and Q_{C3} that energizes the inductor L_c. The discharging operation mode is achieved by turning on the switches Q_{C2} and Q_{C4} and by turning off Q_{C1} and Q_{C3}.The stored energy in the inductor is discharged to the load as a current $I/2$. The circulating current modes occur when the inductor cell deliver a null current to keep a constant current in the inductor cell. Similar operation modes occurred for the negative cycle of the output current waveform.

The inductor cell value can be found from the following equation.

$$L_c = \frac{I_{L_c} R}{f_s \Delta I_{L_c}} \tag{3}$$

Where I_{Lc} is the inductor cell current (in amperes), R is the load resistance (in ohms), f_s is a switching frequency of the inductor cell circuit (in hertz), ΔI_{Lc} is an acceptable current ripple of the inductor cell circuit (in amperes).

In order to filter the harmonic components a filter capacitor is connected across the load

3 Controller and PWM Strategies

A simple Proportional Integral (PI) regulator is applied to control the DC current flowing through the smoothing inductor, which determines the amplitude of the Pulse Width Modulation (PWM) output current waveform I_{PWM} simultaneously. Making the smoothing inductor current follows the reference current is an objective of this current regulator. The switching gate signals of the chopper switch (Q_c) is generated by comparing the error signal of the detected inductor current in the steady state and a triangular waveform after passing through the PI regulator. A schematic control diagram, including the current controller of the chopper and the inductor cell for the five level CSI, is shown in Fig. 2.

The control circuit of the inductor cell functions to control the operation modes, i.e., the charging, the discharging, and the circulating modes, of the inductor cell L_c. The current flowing through the inductor cell I_{Lc} is kept constant. It generates the intermediate level currents based on the output current waveform of the H-bridge CSI. A PI regulator is applied to zero the error between the detected current flowing through the inductor cell and the reference current to obtain stable and balanced intermediate level currents. The amplitude of the inductor cell current is half of the DC input current I_{Li}. The output of the PI regulator is modulated by a triangular carrier to generate the control signal i[0], determining the operation mode of the inductor cell. In case of the nine level CSI, the control circuit of the second inductor cell is similar to the first inductor cell mentioned earlier. The difference is only the reference value of the second inductor cell current I_{Lc2}, which is quarter of the DC input current. Therefore, for an M-level CSI, if the DC current source is assumed to have amplitude I, the current flowing through the Nth inductor cell $I_{Lc(N)}$ is as expressed in (2).

During the maximum and zero levels of the output current generation, there is only circulating current mode, no charging and no discharging operation modes in the inductor cell, as listed in Table 1. The frequency of the triangular carrier waveform determines the switching frequency of the inductor cell's power switches, which also regulates the charging and the discharging modes of the inductor cell. The discharging mode means that the inductor cell injects power to the load, and during the charging mode, the main H-bridge inverter injects power to the load.

Table 1 Possible Switching States of Five Level CSI

Q1	Q2	Q3	Q4	Qc1	Qc2	Qc3	Qc4	Output	Mode of Operation
1	0	0	1	1	1	0	0	0	Circulating Current Mode
1	0	0	1	0	0	1	1	0	Circulating Current Mode
1	0	1	0	1	1	0	0	+I	Circulating Current Mode
1	0	1	0	0	0	1	1	+I	Circulating Current Mode
0	1	0	1	1	1	0	0	-I	Circulating Current Mode
0	1	0	1	0	0	1	1	-I	Circulating Current Mode
1	0	1	0	1	0	1	0	+I/2	Charging Mode
0	1	0	1	0	1	0	1	-I/2	Charging Mode
1	0	0	1	0	1	0	1	+I/2	Discharging Mode
0	1	1	0	1	0	1	0	-I/2	Discharging Mode

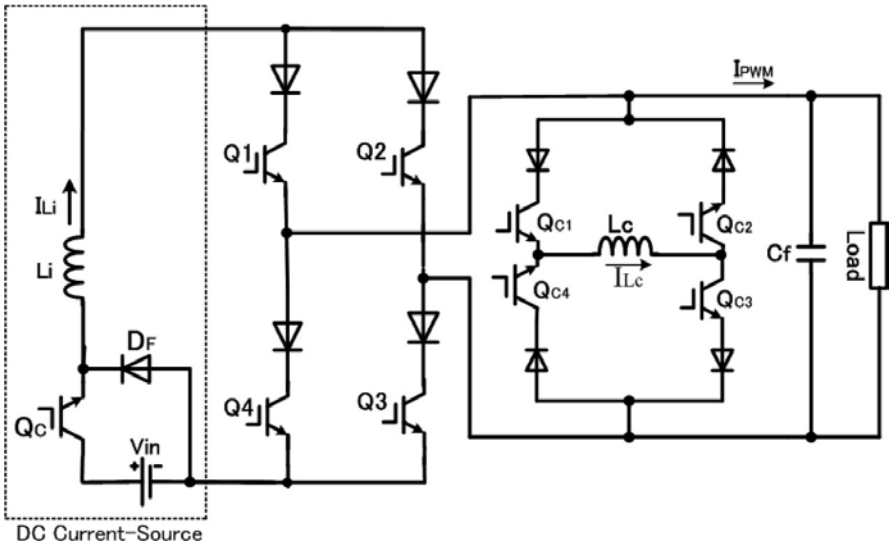

Fig. 1. Five level CSI with chopper based DC current source.

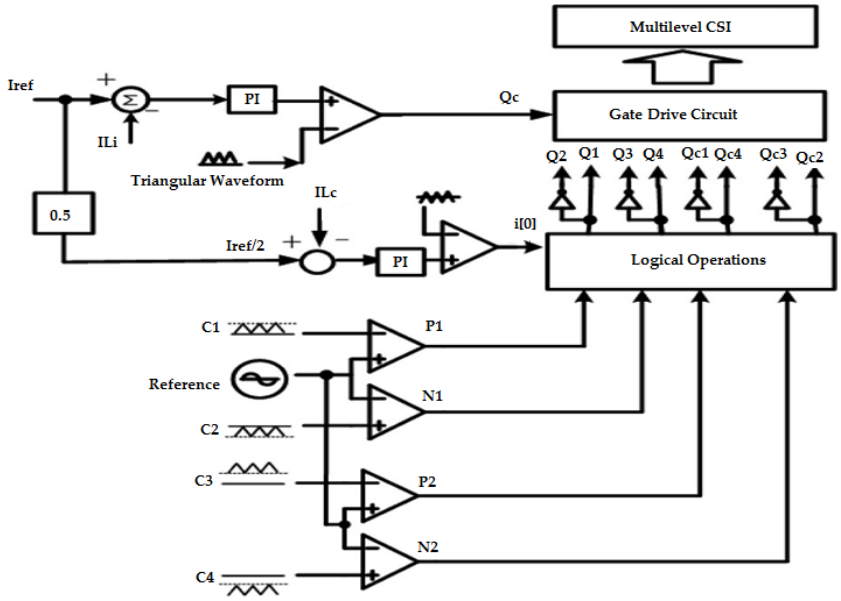

Fig. 2. Control diagram of five level CSI.

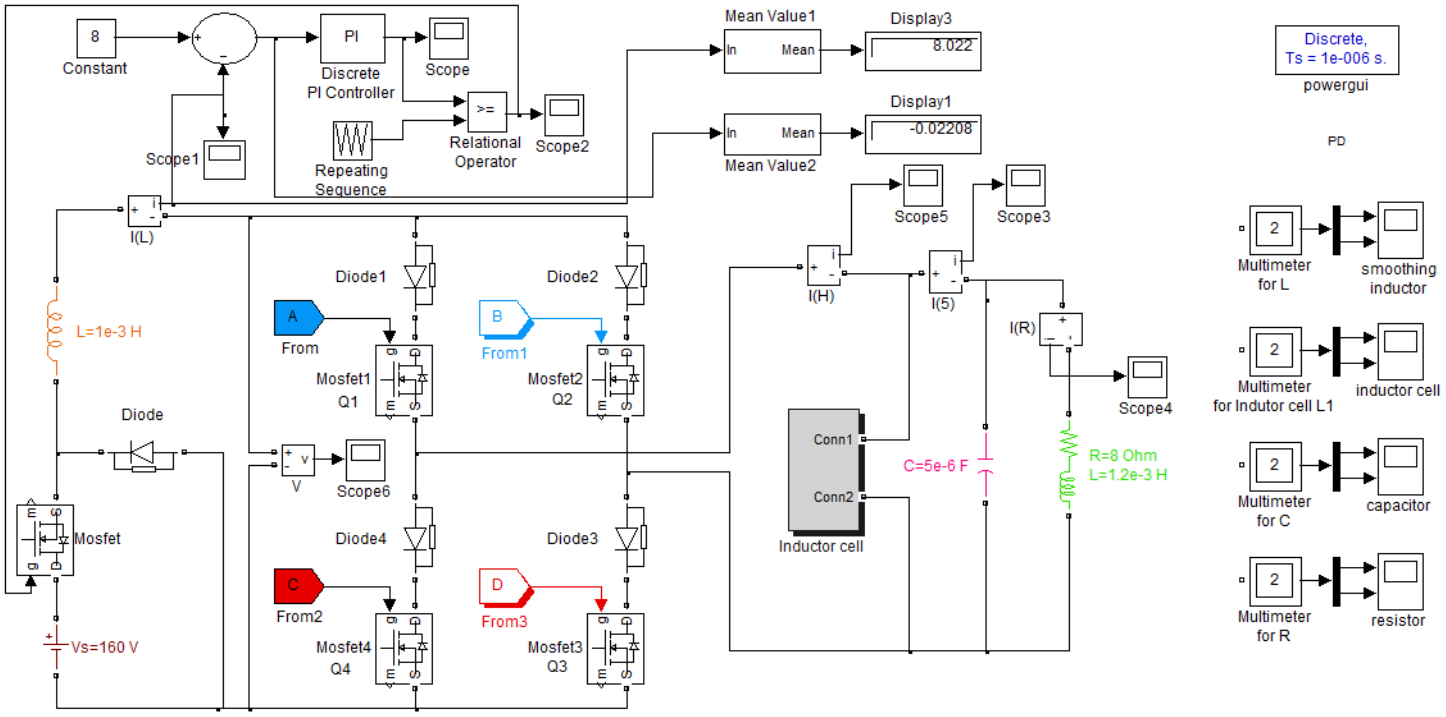

Fig. 3. Five level CSI.

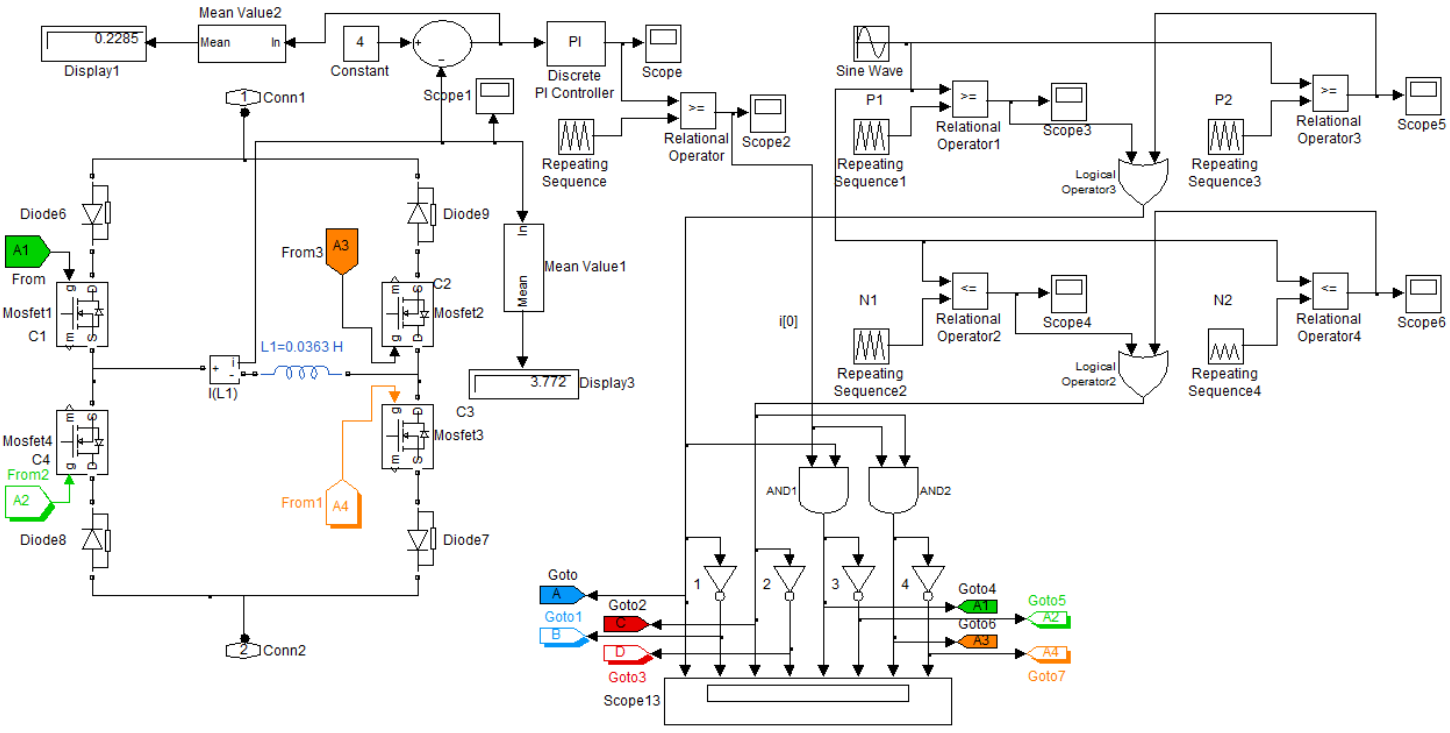

Fig. 4. Inductor cell.

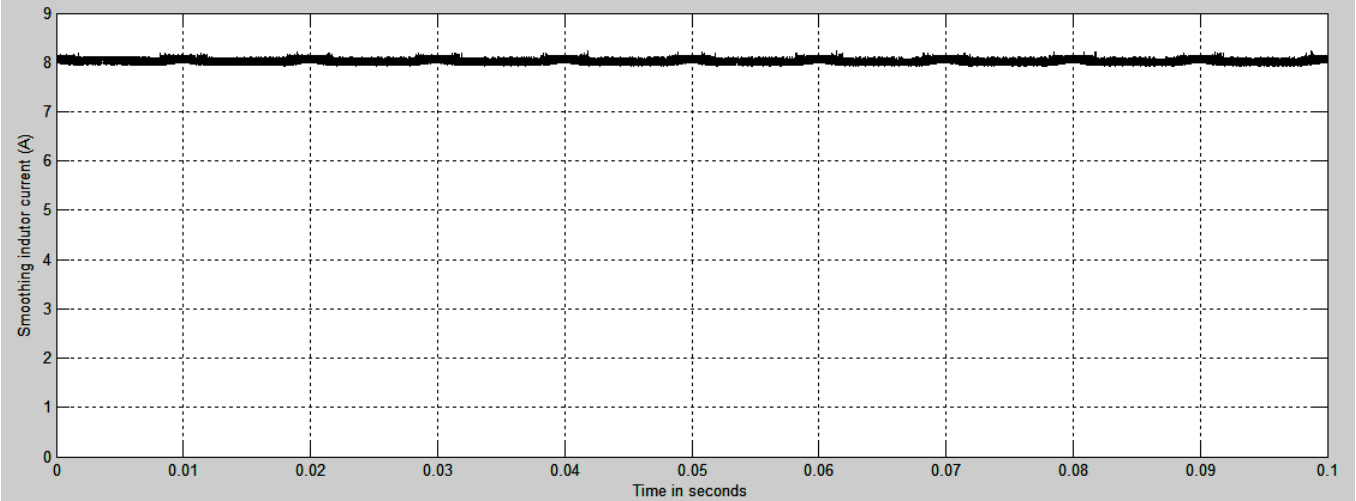

Fig. 5. DC input current.

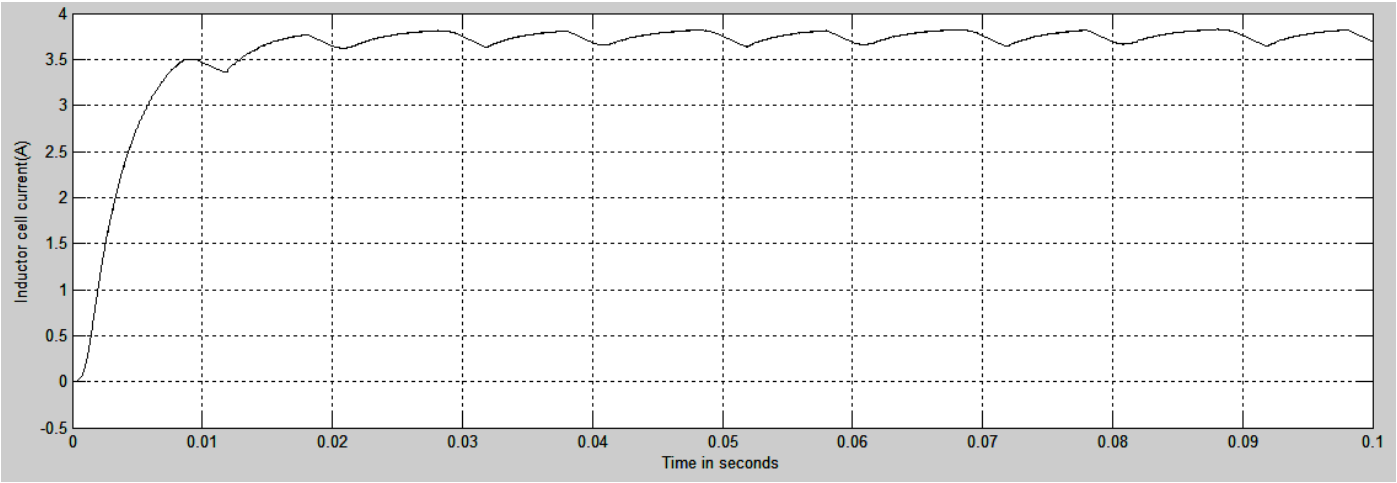

Fig. 6. Inductor cell current.

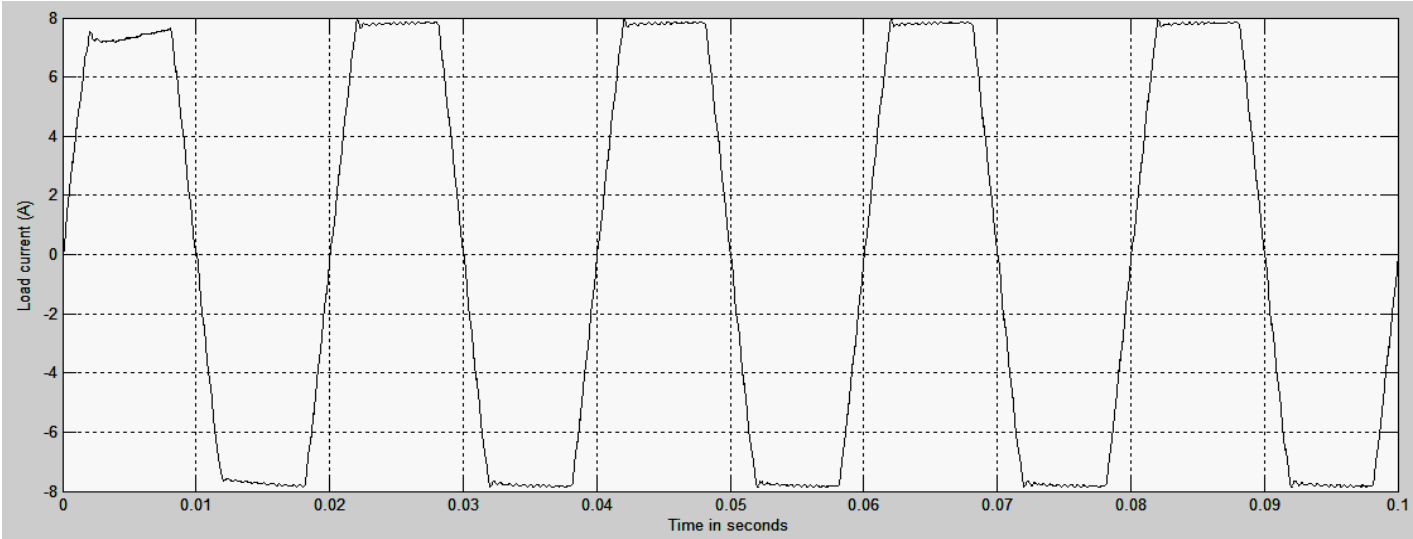

Fig. 7. Load current.

Table 3 Variation of THD for PD Technique.

MODULATION INDEX	THD(%)	RMS(A)	PEAK(A)	DC COMPO-NENT
1	23.58	6.683	9.451	0.06273
0.95	22.32	6.645	9.398	0.06517
0.9	20.9	6.6	9.334	0.06731
0.85	19.46	6.551	9.264	0.06981
0.8	17.69	6.486	9.172	0.06367
0.75	15.74	6.41	9.065	0.06771
0.7	13.49	6.311	8.925	0.08526
0.65	10.96	6.186	8.749	0.08774
0.6	7.98	6.021	8.514	0.09745
0.55	4.57	5.788	8.185	0.1123

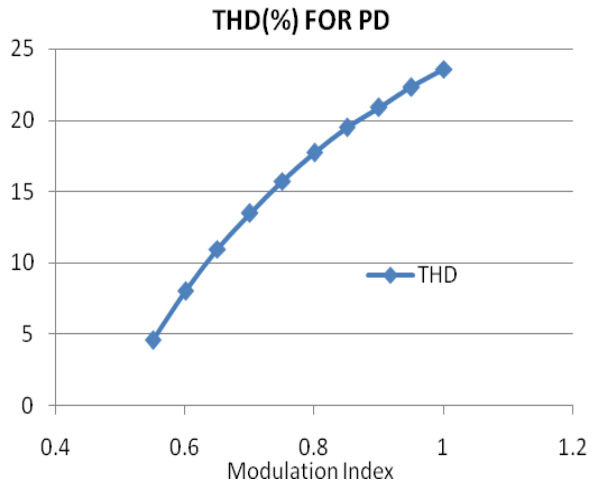

Fig. 8. Plot for PD Technique.

Table 4 Variation of THD for POD Technique.

MODULATION INDEX	THD(%)	RMS(A)	PEAK(A)	DC COMPONENT
1	23.14	6.685	9.455	0.03359
0.95	21.85	6.648	9.401	0.0335
0.9	20.38	6.602	9.336	0.03228
0.85	18.88	6.551	9.265	0.03199
0.8	17.25	6.492	9.18	0.03113
0.75	15.17	6.412	9.067	0.0298
0.7	12.79	6.308	8.92	0.02937
0.65	10.26	6.184	8.745	0.02756
0.6	7.2	6.013	8.504	0.02527
0.55	3.83	5.775	8.167	0.02294

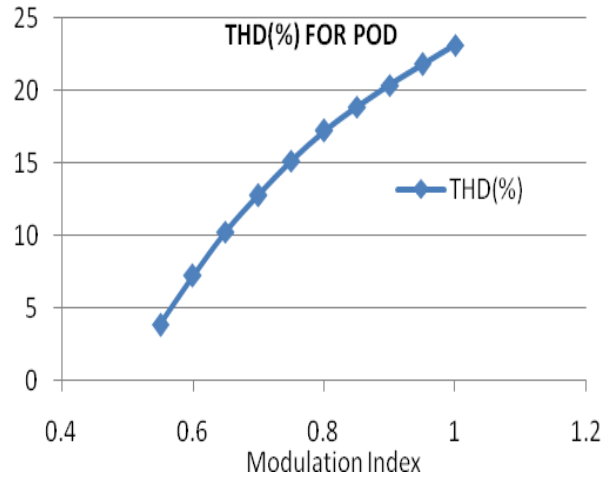

Fig. 9. Plot for POD Technique.

Table 5 Variation of THD for APOD Technique.

MODULATION INDEX	THD%	RMS(A)	PEAK(A)	DC COMPONENT
1	24.11	6.678	9.444	0.03112
0.95	22.9	6.641	9.392	0.02994
0.9	21.52	6.598	9.331	0.02926
0.85	20.17	6.549	9.262	0.02743
0.8	18.27	6.478	9.161	0.02673
0.75	16.47	6.405	9.058	0.02579
0.7	14.42	6.312	8.926	0.0234
0.65	11.92	6.187	8.75	0.02155
0.6	9.13	6.027	8.524	0.01879
0.55	5.9	5.802	8.206	0.01647

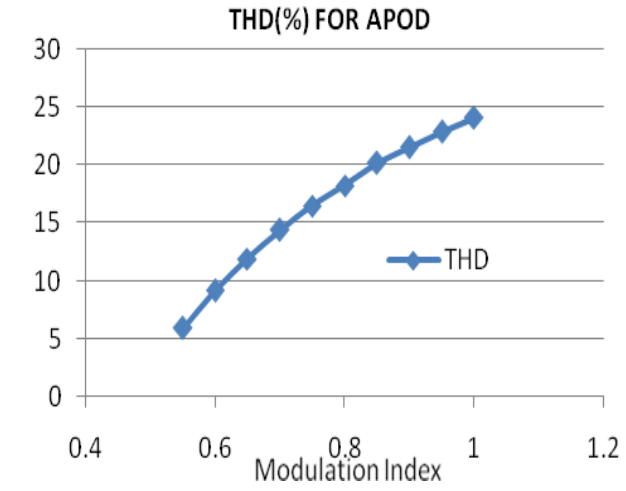

Fig. 10. Plot for APOD Technique.

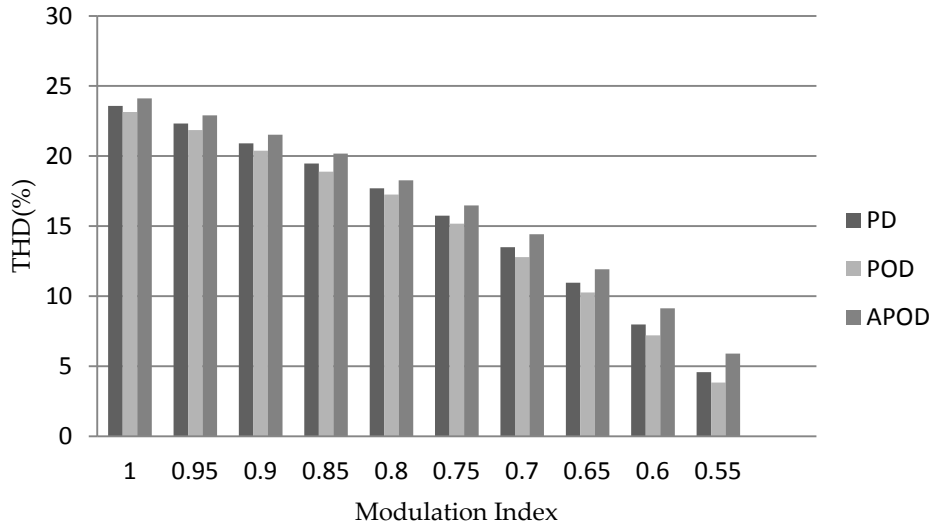

Fig. 11. Comparison Chart for Three Techniques.

In order to achieve a lower distortion of the output current waveform, a PWM technique is applied. In this paper, a level shifted multicarrier based sinusoidal PWM technique is employed to generate gate signals for the CSI power switches and to obtain the PWM current waveforms.

All the generated PWM pulses are given to the gate drive circuit after some logic operations have done.

4 Simulation Results

The new circuit topology of multilevel CSI is examined for a five level CSI configuration. The test parameters are listed in table 2. Partial results are obtained for this test parameter with this new configuration.

Table 2. Test Parameter

Smoothing inductor (L_i) and Inductor cell (L_c)	1mH and 36.3mH
Power source voltage (V_s)	160 V
Inverter switching	22kHz
Filter capacitor (C_f)	5μF
Load	R = 8 Ω , L =1.2mH
Output current frequency	50Hz

Fig. 3 shows the simulation diagram of five level CSI, and the Fig. 4 shows the corresponding inductor cell subsystem. The obtained results are shown in the figures. Fig. 5 shows the DC input current given by the chopper, and the corresponding inductor cell current is shown in fig. 6. Due to the usage of logical operation in generating the gate pulses results in reduced transient period. The output load current is shown in fig. 7.

4.1 Analysis

The intersection of a sine wave with a triangular wave is used to generate firing pulses. There are three alternative strategies to implement this. They are as given below.

- Alternate Phase Opposition Disposition (APOD) - every carrier waveform is in out of phase with its neighbor carrier by 180°.
- Phase Opposition Disposition (POD) - All carrier waveforms above zero reference are in phase and are 180° degree out of phase with those below zero.
- Phase Disposition (PD) - All carrier waveforms are in phase.

In this paper all the three strategies are implemented and the variations are studied on the basis of having lesser THD. The THD value varies, for each Modulation Index (MI) in accordance with the change in PWM strategies. The graphs for all these variations are plotted.

While using the POD technique along with logical operations in generating gate pulses, this new configuration is working well and having lesser THD value when compared to PD and APOD techniques.

5 Conclusion

A new configuration of multilevel CSI, which employs inductor cells as auxiliary circuit, has been used with simple PI controller. The inductor cells are connected in parallel with the main H-bridge CSI to generate multilevel output current waveforms without additional external DC power sources.

Three level shifted multicarrier based sinusoidal PWM techniques are used in the controller and found that the POD is the best PWM technique to this new configuration, and the usage of logical operations results in reduced transient period.

The proposed topology has been verified through Matlab Simulation.

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